PTO-1390 (Modified) (5-2000) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTORNEY'S DOCKET NUMBER 86397
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR) 10/049875
INTERNATIONAL APPLICATION NO. PCT/JP00/05738	INTERNATIONAL FILING DATE AUGUST 25, 2000	PRIORITY DATE CLAIMED AUGUST 27, 1999

TITLE OF INVENTION

Silicon Wafer and Method For Manufacturing Thereof, and Method For Evaluation of Silicon Wafer

APPLICANT(S) FOR DO/EO/US

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Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (24) indicated below.
4. ☐ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☒ is attached hereto (required only if not communicated by the International Bureau).
   b. ☐ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
10. ☐ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).
11. ☐ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☒ A copy of the International Search Report (PCT/ISA/210).

Items 13 to 20 below concern document(s) or information included:

13. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
20. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
21. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
22. ☒ Certificate of Mailing by Express Mail
23. ☒ Other items or information:

    an application data sheet

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
10/049875	PCT/JP00/05738	86397

24. The following fees are submitted:.	CALCULATIONS	PTO USE ONLY
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :		
☐ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO $1040.00		
☒ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO $890.00		
☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO $740.00		
☐ International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) $710.00		
☐ International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) $100.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$890.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).	$0.00	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	8 - 20 =	0	x $18.00	$0.00	
Independent claims	5 - 3 =	2	x $84.00	$168.00	
Multiple Dependent Claims **(check if applicable)**.			☐	$0.00	
TOTAL OF ABOVE CALCULATIONS =				$1,058.00	
Applicant claims small entity status. See 37 CFR 1.27). The fees indicated above are reduced by 1/2.				$0.00	
SUBTOTAL =				$1,058.00	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). +				$0.00	
TOTAL NATIONAL FEE =				$1,058.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).** ☒				$40.00	
TOTAL FEES ENCLOSED =				$1,098.00	
				Amount to be: refunded	$
				charged	$

a. ☒ A check in the amount of **$1,098.00** to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of _____ to cover the above fees. A duplicate copy of this sheet is enclosed.

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NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

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NAME

27,466
REGISTRATION NUMBER

02/12/2002
DATE

86397

PATENT #4/a

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re U.S. Patent Application)
)
Applicants: Satoshi Komiya, Shiro Yoshino)
Masayoshi Danbata and)
Kouichirou Hayashida)
)
Serial No.: Not Yet Assigned)
)
Filed: Herewith)
)
For: **Silicon Wafer and Method For Manufacturing**)
Thereof, and Method)
For Evaluation of Silicon Wafer)

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This is a Preliminary Amendment for entry in the above-identified application.

In the Claims:

Please amend claims 3 and 5 as follows:

3. (amended) A silicon wafer for non-oxidative heat treatment for use in semiconductor device manufacture according to claim 1, wherein the silicon wafer is a silicon wafer for hydrogen heat treatment or a silicon wafer for argon annealing.

5. (amended) A silicon wafer for manufacturing a semiconductor device manufactured by hydrogen heat treatment or argon annealing of the silicon wafer for non-oxidative heat treatment according to claim 1.

Respectfully submitted,

Date: February 12, 2002

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

3. (amended) A silicon wafer for non-oxidative heat treatment for use in semiconductor device manufacture according to [any of claim 1 and claim 2] claim 1, wherein the silicon wafer is a silicon wafer for hydrogen heat treatment or a silicon wafer for argon annealing.

5. (amended) A silicon wafer for manufacturing a semiconductor device manufactured by hydrogen heat treatment or argon annealing of the silicon wafer for non-oxidative heat treatment according to [any one of claims 1 to claim 3] claim 1.

DESCRIPTION

SILICON WAFER AND METHOD FOR MANUFACTURE THEREOF, AND METHOD FOR EVALUATION OF SILICON WAFER

TECHNICAL FIELD

The present invention relates to a method of manufacturing silicon wafers to be used in manufacturing semiconductor devices, suitable for non-oxidative heat treatment such as for example hydrogen atmosphere high-temperature heat treatment (called hydrogen heat treatment) etc.

BACKGROUND ART

Void defects etc that are agglomerated by vacancies and detected as for example LSTD, FPD or COP are present in silicon wafers (CZ-silicon wafers) manufactured by the Czochralski method (hereinbelow referred to as the CZ method). Since such crystal defects have an adverse effect on the quality of the final product, heat treatment such as hydrogen atmosphere high-temperature heat treatment (also called hydrogen heat treatment or hydrogen annealing) is often performed in order to remove such crystal defects. In fact it is known (Examined Japanese Patent Publications 3-80338) that in CZ-silicon wafers subjected to hydrogen treatment, void defects agglomerated by vacancies detected as LSTDs etc are eliminated, with the result that excellent oxide film voltage-withstanding properties are displayed.

However, since there is the problem that the benefit of hydrogen heat treatment is restricted exclusively to the extreme surface vicinity of the wafer,

and noting the fact that the defect-eliminating benefit by the hydrogen heat treatment increases as the defect size becomes smaller, the method has been proposed (Unexamined Japanese Patent Publication No.10-208987) of extending the benefit of the hydrogen heat treatment to deeper regions by speeding up the rate of cooling in the temperature zone where defects are generated during crystal growth so as to reduce the size of the defects to a very small size and performing hydrogen heat treatment thereon.

In addition, in order to make it possible to cope with increase in crystal diameter by this method, a method has also been proposed (Unexamined Japanese Patent Publication No.10-260666) of achieving good wafer quality by optimizing V/G (where V is the pulling speed and G is the temperature gradient in the axial direction of the crystal in the vicinity of the melting-point), which governs the concentration of point defects (voids), which are thought to be the source of defects.

Recently, as another approach relating to reducing the size of defects, it is reported (Unexamined Japanese Patent Publication No.10-98047) that wafers suitable for annealing can be manufactured by reducing the defect size by addition of nitrogen during growth of CZ silicon single crystals.

However, when nitrogen is added during crystallization from the melt, the nitrogen concentration changes in the length direction of the crystal due to segregation, so the problem arises that this tends to cause a nonuniform distribution of defects as a result.

Furthermore, although it is true that, when nitrogen is added, the benefit of high-temperature annealing can be more easily manifested, due to decrease in defect size. However, since the defect density increases on the other hand,

under inadequate high-temperature annealing conditions, there is contrariwise a risk of causing deterioration of wafer quality.

To summarize, it has still not yet been fully verified whether or not wafers in which defect size has been reduced by addition of nitrogen (nitrogen doping) as described above are indeed suitable for use as products, and it has in fact not yet been clarified whether nitrogen-doped wafers can indeed be used as wafers for semiconductor device manufacture or not.

DISCLOSURE OF THE INVENTION

The present invention has been made in view of the foregoing problems, and an object of the present invention is, in a method of manufacturing a silicon wafer by doping with nitrogen, to verify manufacturing conditions such that a silicon wafer having satisfactory properties for use as a semiconductor device can be manufactured, and to enable manufacture of a nitrogen-doped wafer having excellent characteristics as a wafer for manufacturing a semiconductor device after performing heat treatment.

As a result of detailed study of growth conditions in view of the aforementioned problems, the inventors of the present application discovered manufacturing conditions for silicon wafers that have fully satisfactory performances for use in advanced semiconductor devices even after heat treatment, and thereby perfected the present invention.

More specifically, when the present inventors evaluated wafer performance through the measurement of gate oxide integrity of wafers doped with nitrogen (nitrogen-doped wafers), they discovered that, with this process, while nitrogen-doped wafers tended to show excellent results in a TZDB (time zero dielectric breakdown) test compared with wafers that had not been

subjected to nitrogen doping after heat treatment under a non-oxidizing atmosphere, if the wafers were doped with nitrogen to a high concentration, the results of the TDDB (time dependent dielectric breakdown) test showed abnormalities.

Also, the present inventors discovered that, whereas whether the TZDB test results are good or not and whether abnormalities appear in the TDDB test results or not depend on the nitrogen concentration of the nitrogen-doped wafer, at the same time, the TZDB test results depend on the type of gas with which non-oxidative heat treatment is performed (for example whether this is hydrogen gas or argon gas), yet the nitrogen concentration for which abnormalities appear in the TDDB test results does not depend on the type of gas which is used to perform the non-oxidative heat treatment, but, rather, can be inferred to be practically fixed.

With these discoveries that made a great contribution to perfecting the present invention, the present inventors present for the first time in the present application the fact that nitrogen-doped wafers containing nitrogen of concentration not more than 4×10^{14} atoms/cm^3, which is a concentration at which abnormalities appear in the TDDB test after heat treatment under non-oxidative atmosphere, are preferable as silicon wafers for non-oxidative heat treatment for semiconductor device manufacture. They therefore have taken this as the basic content of the claims of the present application.

Also, when nitrogen-doped wafers were evaluated in terms of the non-defective ratio with respect to gate oxide film voltage-withstand properties (GOI), the benefit of hydrogen heat treatment was fully displayed at the surface. In addition this benefit was independent of the amount of nitrogen doping. However, when an evaluation was conducted regarding a portion at a certain

depth, the gate oxide film non-defective ratio was found to depend on nitrogen concentration and in fact there is an upper limit and a lower limit for the nitrogen doping amount. Thus it became clear that, when used as a product for a semiconductor device, the nitrogen concentration must be within a prescribed range. This discovery also contributed greatly to perfecting the present invention.

It should be noted that although the aforementioned Unexamined Japanese Patent Publication No. 10-98047 has the statement "a nitrogen concentration of at least 1 X 10^{14} atoms/cm^3", no information in support of this is disclosed.

More specifically, according to the present invention, methods as indicated below and silicon wafers for non-oxidative heat treatment for semiconductor device manufacture are proposed.

A silicon wafer for non-oxidative heat treatment for semiconductor device manufacture wherein the nitrogen concentration is in the range from 5 X 10^{13} atoms/cm^3 to 1 X 10^{15} atoms/cm^3, preferably the range from 5 X 10^{13} atoms/cm^3 to 8 X 10^{14} atoms/cm^3, even more preferably 5 X 10^{13} atoms/cm^3 to 4 X 10^{14} atoms/cm^3 and further more preferably the range from 1 X 10^{14} atoms/cm^3 to 4 X 10^{14} atoms/cm^3.

Specifically, considering only the gate oxide film voltage-withstanding capability as found by TZDB, the range of nitrogen concentration for a good quality product corresponds to from 5 X 10^{13} atoms/cm^3 to 1 X 10^{15} atoms/cm^3 (within a range of gate oxide film withstand-voltage non-defective ratio of at least 90% as found by TZDB), preferably within a range of nitrogen concentration of 1 X 10^{14} atoms/cm^3 to 8 X 10^{14} atoms/cm^3 (within a range of gate oxide film withstand-voltage non-defective ratio of at least 95% as found

by TZDB); if, in addition, the fixed current value TDDB is taken into consideration, this must be 4 X 10^{14} atoms/cm^3 or less. The range for satisfactory products can therefore be divided into four, namely, a range of from 5 X 10^{13} atoms/cm^3 to 1 X 10^{15} atoms/cm^3; a range of 5 X 10^{13} atoms/cm^3 to 8 X 10^{14} atoms/cm^3; a range of from 5 X 10^{13} atoms/cm^3 to 4 X 10^{14} atoms/cm^3; and a range of from 1 X 10^{14} atoms/cm^3 to 4 X 10^{14} atoms/cm^3. These are suitably selected in accordance with the product to be manufactured.

It should be noted that the types of silicon wafer for heat treatment may include silicon wafers for hydrogen heat treatment supplied for heat treatment under a hydrogen atmosphere, silicon wafers for argon heat treatment supplied for heat treatment under an argon atmosphere, or silicon wafers for mixed gas supplied for heat treatment under a mixed gas atmosphere of hydrogen and argon; however, all non-oxidative heat treatments for reducing crystal defects of the wafer surface layer (annealing treatments under conditions in the absence of oxygen) are included in the scope of the present invention.

In a method of manufacturing a silicon ingot by pulling a silicon single crystal by the Czochralski method, a method of manufacturing a silicon ingot by pulling a silicon single crystal under conditions such as to form a portion of nitrogen concentration from 5 X 10^{13} atoms/cm^3 to 4 X 10^{14} atoms/cm^3 by doping of nitrogen. In particular, in a method of manufacturing a silicon ingot by pulling a silicon single crystal by the Czochralski method, a method of manufacturing a silicon ingot for manufacturing silicon wafers for non-oxidative heat treatment by pulling a silicon single crystal under conditions such as to form a portion of nitrogen concentration from 1 X 10^{14} atoms/cm^3 to 4 X 10^{14} atoms/cm^3 by doping of nitrogen.

In one embodiment of the present invention, a silicon wafer for heat treatment for semiconductor device manufacture as described above is manufactured by the Czochralski method (CZ method). In this case, a silicon ingot was manufactured by the Czochralski method by pulling a silicon single crystal while doping with nitrogen so as to provide a nitrogen concentration in a portion or the whole thereof of 5×10^{13} to 1×10^{15} atoms/cm^3. Then, a portion of nitrogen concentration in the range 5×10^{13} to 1×10^{15} atoms/cm^3, preferably 1×10^{14} atoms/cm^3 to 8×10^{14} atoms/cm^3 was cut from this silicon ingot and used for a silicon wafer for non-oxidative heat treatment for semiconductor device manufacture and in particular for a silicon wafer for hydrogen heat treatment or a silicon wafer for argon annealing. If the CZ method is employed, a system in which a magnetic field is applied to the melt (MCZ method) may also be adopted.

As the method of nitrogen doping, all methods that are currently known, such as the method of admixing nitrogen with the argon gas that is passed through the furnace when growing the crystal or the method of introducing nitrogen atoms into the pulled single crystal by dissolving silicon nitride in the raw-material melt and all methods that may in future be discovered can be employed.

Also, as embodiments of the present invention, the following may be cited.

A silicon wafer for semiconductor device manufacture manufactured by performing hydrogen heat treatment or argon annealing on a silicon wafer (silicon wafer for non-oxidative heat treatment as referred to above) for non-oxidative heat treatment for semiconductor device manufacture according to the present invention.

A silicon wafer for semiconductor device manufacture wherein the amount of nitrogen doping is adjusted taking into account the life of a virtual element.

A method of evaluating a nitrogen-doped wafer characterized in that a decision is made as to whether or not this nitrogen-doped wafer can be employed as a wafer for semiconductor device manufacture by calculating the life of a virtual element on the nitrogen-doped heat-treated wafer.

A method of evaluating a wafer as set out above characterized in that the method of calculating the life of a virtual element on the aforementioned wafer is a TDDB test.

By "virtual element" is meant a simulated element structure manufactured when performing a TDDB test or TZDB test; by "life of a virtual element" is meant the life of this simulated element structure.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a graph illustrating the relationship between added nitrogen concentration and oxide film withstand-voltage non-defective ratio after hydrogen annealing;

Figure 2 is a graph illustrating the relationship between added nitrogen concentration and oxide film withstand-voltage non-defective ratio after removal of a 3 μm surface layer by polishing after hydrogen annealing;

Figures 3(A) and 3(B) are views illustrating the measurement results of a silicon wafer constant-current TDDB test after hydrogen heat treatment. Figure 3(A) is a view illustrating the measurement results of a constant-current TDDB test of a normal element in which nitrogen doping is not performed and Figure 3(B) is a view illustrating the measurement results of a constant-current TDDB

test of an element wherein no abnormalities were produced by performing nitrogen doping at high concentration;

Figures 4(A) and 4(B) are views showing the results of measurement of the gate oxide film withstand-voltage (GOI) obtained by a TZDB test of an argon-annealed nitrogen-doped wafer. In Figure 4, Figure 4(A) is a view showing the case where polishing was not performed, the case after 3 μm polishing, and the case after 6 μm polishing respectively superimposed; Figure 4(B) is a view showing only data for the case of 3 μm polishing in particular, in order to facilitate understanding of the difference in comparison with Figure 2, which shows the case of 3 μm polishing after performing hydrogen annealing;

Figures 5(A) through 5(D) are views showing the results of a constant-current TDDB test of an argon-annealed nitrogen-doped wafer. In particular, Figure 5(A) to Figure 5(D) are views showing the results of a constant-current TDDB test in which, from a condition (Figure 5 (A)) in which no doping at all with nitrogen is performed, the nitrogen concentration was raised to 5×10^{13} atoms/cm^3 (Figure 5 (B)), 1×10^{14} atoms/cm^3 (Figure 5(C)), and 1.13×10^{14} atoms/cm^3 (Figure 5(D));

Figures 6(A) through 6(D) are views showing the results of a constant-current TDDB test of an argon-annealed nitrogen-doped wafer. In particular, Figure 6(A) to Figure 6(C) are views showing the results of a constant-current TDDB test in which the nitrogen concentration was raised to 1.64×10^{14} atoms/cm^3 (Figure 6(A)), 5.82×10^{14} atoms/cm^3 (Figure 6 (B)), and 1.37×10^{15} atoms/cm^3 (Figure 6(C)). Figure 6(D) shows respectively hydrogen-annealed and argon-annealed wafers superimposed, doped with nitrogen at 5.82×10^{14} atoms/cm^3 and at 1.37×10^{15} atoms/cm^3;

Figure 7 is a view showing the results of Figure 5(A) to Figure 6(C) superimposed; and

Figure 8 is a view showing changes in nitrogen concentration in a single crystal pulled using the CZ method.

BEST MODE FOR CARRYING OUT THE INVENTION

As test examples, the present inventors cut silicon wafers from a CZ-silicon single crystal grown under various conditions and examined the effectiveness of defect elimination in the wafer depth direction by performance of hydrogen annealing after performing specular polishing process.

<Growing single crystals>

The crystals with boron added as dopant and diameter 200 mm, of p type and crystal orientation <100> were grown with the factors that control defect behavior, namely, V/G1 and V X G2 respectively in the ranges 0.13 to 0.4 $mm^2/min°C$ and 0.5 to 10°C/min (where V is the pulling speed, G1 is the temperature gradient in the vicinity of the solid/liquid interface, and G2 is the temperature gradient of the temperature zone of defect formation).

<Nitrogen doping>

In growing such silicon single crystal ingots, nitrogen addition was performed such as to produce a nitrogen concentration of 4.9×10^{13} atoms/cm^3 to 1.24×10^{15} atoms/cm^3. Also, for comparison, crystals were prepared without nitrogen addition.

The nitrogen addition was performed by the method of introducing nitrogen gas into the CZ furnace or the method (Unexamined Japanese Patent Publication No.5-294780) of mixing with the raw-material silicon a wafer formed with a silicon nitride film on its surface.

<Quantitative determination of nitrogen concentration>

For the quantitative determination of nitrogen concentration, quantitative determination was performed in respect of the portions capable of measurement using SIMS by measurement using SIMS, and, in respect of the portions incapable of measurement using SIMS, quantitative determination was performed from the portions measured using SIMS by calculation using a prescribed calculation formula.

More specifically, quantitative determination was performed on the extreme tail portion of the crystal straight cylindrical portion (solidification ratio about 90%) having a concentration of nitrogen sufficiently larger than the minimum value for detection in quantitative determination of nitrogen (up to 1 X 10^{14} atoms/cm^3) using SIMS (manufactured by Cameca, model IMF-6F).

It was confirmed that there was no external disturbance to the measured values due to residual nitrogen gas from the atmosphere entering during sample changeover by using a silicon crystal grown by the FZ method, in which nitrogen was not introduced, as blank. Also, quantitative determination was performed with the nitrogen concentration calibrated by a known standard sample formed by ion implantation of nitrogen.

The nitrogen concentration in positions which could not be measured using SIMS was calculated using the following calculation formula.

$$Cs = kCo(1 - L)^{k-1}$$

Where Cs is the impurity concentration in the crystal, Co is the initial impurity concentration in the melt, L is the solidification ratio and K is the segregation coefficient of nitrogen, taken to be 0.0007, from the reference: Yatsurugi et al (1973) J. Electrochem. Soc. 120. 975, which is well used in this field of industry.

In the above calculation formula, the concentration of nitrogen impurity in the molten silicon which is taken into the crystal is expressed using the segregation coefficient k which is characteristic of the impurity.

The formula given above is a formula which expresses the segregation phenomenon. Due to the segregation phenomenon, the impurity concentration (nitrogen concentration) increases with growth of the crystal, becoming a high concentration at the extreme tail portion of the crystal straight cylindrical portion, at which the minimum value for detection in quantitative determination of nitrogen by SIMS (up to 1 X 10^{14} atoms/cm^3) is exceeded.

For the above reasons, in this practical example, it is arranged to measure the nitrogen concentration by SIMS at the extreme tail portion (solidification ratio about 90%) of the crystal straight cylindrical portion and the concentration at each crystal position is then calculated from the above formula using this value.

<Wafer heat treatment>

After doping with nitrogen ascribed above, hydrogen heat treatment (hydrogen annealing) and argon annealing were performed on a wafer that had been subjected to the quantitative determination process. Regarding the hydrogen annealing conditions and argon annealing, typically processing was performed at 1200 °C X 1 hour and the gate oxide film withstand-voltage characteristic (GOI) was examined in a condition immediately after hydrogen heat treatment and immediately after argon annealing, respectively, in a condition in which 3 μm of the surface layer was removed after hydrogen treatment and a condition in which 3 μm of the surface layer was removed after argon annealing.

< Evaluation of hydrogen heat-treated (hydrogen-annealed) wafer>

[Gate oxide film withstand-voltage (GOI)]

The gate oxide film withstand-voltage was measured by forming a MOS structure on a wafer and applying voltage thereto. When measuring the gate oxide film withstand-voltage after polishing to a depth of 3 μm, the wafer surface was polished to a depth of about 3 μm and the measurement was made by forming a MOS structure thereon and applying voltage thereto.

[TZDB (Time Zero Dielectric Breakdown) test]

When measuring gate oxide film withstand-voltage by TZDB, in the case of the measurement method adopted in this test example, polysilicon electrodes of 10 mm^2 were used as gate electrodes and voltage was applied thereto by the step voltage application method. Also, the oxide film thickness was 25 nm. Furthermore, the measurement temperature was room temperature (25°C), and the withstand-voltage evaluation current was 10 μA.

As a result, as shown in Figure 1, the oxide film withstand-voltage non-defective ratio immediately after hydrogen treatment was practically 100%, irrespective of nitrogen concentration and growth conditions.

However, when, after hydrogen treatment, the surface layer of 3 μm was removed and the oxide film withstand-voltage ascertained, as shown in Figure 2, it was found that, although non-defective ratio increased with increase in nitrogen concentration up to 6 X 10^{14} atoms/cm^3, above this, the non-defective ratio actually fell.

Taking into consideration integrity of the wafer surface layer (device active layer), whose importance increases as the integration degree of device becomes higher, it is necessary to maintain an oxide film withstand-voltage non-defective ratio as far as a depth of 3 μm from the surface layer of at least 90%.

From Figure 2 it can therefore be seen that in order to achieve an oxide film withstand-voltage non-defective ratio of 90% or more it is necessary that the nitrogen concentration should be in the range 5×10^{13} to 1×10^{15} atoms/cm^3; and, in order to achieve an oxide film withstand-voltage non-defective ratio of 95% or more, which is even more preferable for the product, it can be seen that it is necessary to set the nitrogen concentration in the range 1×10^{14} to 8×10^{14} atoms/cm^3.

[Constant-current TDDB (time dependent dielectric breakdown) test]

For the constant-current TDDB, breakdown of the oxide film after lapse of a prescribed time with the current kept constant is ascertained by change of the voltage applied to the element. For measurement, a MOS structure is formed in the same way as in the case of inspection of the oxide film withstand-voltage.

In the measurement, with the method of measurement adopted in this test example, polysilicon electrodes of 1 mm^2 were used as the electrodes. Also, the oxide film thickness was 25 nm. Furthermore, the measurement temperature was 125°C, the applied current density was 50 mA/cm^2, and the evaluating electrical field was 4 MV/cm.

When the constant-current TDDB was measured, it was found that, in the case of a normal element, instantaneous breakdown occurred on exceeding about 100 seconds. However, in the case of an abnormal element, instantaneous breakdown did not occur but rather breakdown occurred over time, so breakdown proceeded progressively, starting from before the lapse of 100 seconds. Consequently, the result is that breakdown is observed to have occurred after lapse of 100 seconds, depending on the value to which the evaluating electrical field is set. Consequently, if the measurement results of

constant-current TDDB are graphed, in the case of normal elements, the results are concentrated on the plot at a location after lapse of a fixed time (in this case, about 100 seconds) and points on the plot do not appear elsewhere (see Figure 3(A)); however, in the case of abnormal elements, points on the plot do appear elsewhere at locations remote from a lapsed time of 100 seconds (see Figure 3(B)).

Occurrence of such abnormalities in heat-treated wafers is not observed in wafers that have been heat-treated with no nitrogen doping (Figure 3(A)), but is a characteristic phenomenon occurring in respect of heat-treated wafers that have been doped with nitrogen to a high concentration.

The TDDB test is one type of reliability test of semiconductor devices and provides an index of the constancy of the ability to withstand element fatigue. The TDDB test can also be utilized to provide simulated data for inferring stability of the life of semiconductor devices manufactured from the wafers used in the test.

In this test example, the constant-current TDDB in a condition in which no polishing was performed and the constant-current TDDB after polishing to a depth of 3 μm were measured for various wafers after hydrogen heat treatment.

As a result, the data shown in the tables below were obtained.

[Table 1]

Item evaluated / Nitrogen concentration (atoms/cm^3)	TDDB abnormality ratio %
0	0
0	0
0	0
0	0
5.00E+13	0
5.10E+13	0
6.30E+13	0
1.13E+14	0
1.41E+14	0
1.51E+14	0
1.64E+14	0
4.97E+14	21.6
5.82E+14	7.35
6.48E+14	29.7
1.26E+15	5.41
1.37E+15	8.82

[Table 2]

Item evaluated / Nitrogen concentration (atoms/cm^3)	TDDB abnormality ratio %
0	0
0	0
0	0
0	0
5.00E+13	0
5.10E+13	0
6.30E+13	0
1.13E+14	0
1.41E+14	0
1.51E+14	0
1.64E+14	0
4.97E+14	18.9
6.48E+14	8.11
8.61E+14	13.5
1.12E+15	10.8
1.26E+15	8.11

Table 1 shows the relationship between the nitrogen concentration in the condition in which no polishing is performed and the constant-current TDDB

abnormality ratio; Table 2 shows the relationship between the nitrogen concentration after polishing to 3 μm and the constant-current TDDB abnormality ratio. As shown in these tables, normal values of the constant-current TDDB are shown when the nitrogen concentration is 4×10^{14} atoms/cm^3 or less. Consequently, by adding this requirement to the aforementioned oxide film withstand-voltage conditions, the optimum conditions for a nitrogen-doped crystal become such as to provide a silicon wafer for heat treatment wherein the nitrogen concentration is in a range from 5×10^{13} atoms/cm^3 to 4×10^{14} atoms/cm^3, in particular, a silicon wafer for heat treatment wherein the nitrogen concentration is in a range from 1×10^{14} atoms/cm^3 to 4×10^{14} atoms/cm^3.

<Evaluation of argon-annealed wafer>

[TZDB (time zero dielectric breakdown) test]

Measurement of the gate oxide film withstand-voltage (GOI) using the TZDB test was conducted under the same conditions as in the case of hydrogen annealing. However, in the case of argon annealing, the gate oxide film withstand-voltage was also measured after polishing to 6 μm. The results are shown in Figure 4. It should be noted that, whereas, in this Figure 4, Figure 4(A) shows the case where polishing was not performed, the case where polishing to 3 μm was performed and the case where polishing to 6 μm was performed, respectively superimposed, in Figure 4(B), in order to facilitate understanding of the difference from Figure 2, which shows the case where polishing to 3 μm was performed after hydrogen annealing, in particular only data for the case of polishing to 3 μm are shown.

As can be seen from this Figure 4, wafers that have been subjected to nitrogen doping have excellent gate oxide film withstand-voltage

characteristics in the TZDB test, compared with wafers that have not been subjected to nitrogen doping; also, no clear upper limit is observed as it is in the case of wafers polished to a depth of 3 μm after hydrogen annealing. Consequently, in the case of argon-annealed wafers that have been subjected to nitrogen doping either nothing like an upper limit in regard to nitrogen concentration is found in the TZDB test, or an upper limit is found at a location appreciably higher than the nitrogen concentration of 1×10^{15} atoms/cm^3, which is the upper limit in the case of hydrogen annealing. Furthermore, as can be seen from Figure 4(A), there is not much difference in the results of the TZDB test for argon-annealed wafers both in the case of wafers that were polished to a depth of 3 μm and wafers that were polished to a depth of 6 μm.

[Constant-current TDDB (time dependent dielectric breakdown) test]

The constant-current TDDB test also, like the TZDB test, was conducted under the same conditions as in the case of hydrogen annealing. The results are shown in Figure 5 to Figure 7.

Figure 5 and Figure 6 show the results of a constant-current TDDB test when the nitrogen concentration was raised from a condition in which no nitrogen doping at all was performed (Figure 5(A)) to 5×10^{13} atoms/cm^3 (Figure 5(B)), 1×10^{14} atoms/cm^3 (Figure 5(C)), 1.13×10^{14} atoms/cm^3 (Figure 5(D)), 1.64×10^{14} atoms/cm^3 (Figure 6(A)), 5.82×10^{14} atoms/cm^3 (Figure 6(B)), and 1.37×10^{15} atoms/cm^3 (Figure 6(C)).

As is clear from these Figures, although, up to a nitrogen concentration of 1.64×10^{14} atoms/cm^3 (Figure 6(A)), the densely concentrated condition of the points on the graph is unchanged, when the nitrogen concentration is 5.82×10^{14} atoms/cm^3 (Figure 6(B)) or 1.37×10^{15} atoms/cm^3 (Figure 6(C)), the

shifting of the points on the graph to locations somewhat to the rear of 100 seconds which is characteristic of abnormal elements appears.

In Figure 6(D), the results obtained with wafers doped with nitrogen with a concentration of 5.82×10^{14} atoms/cm^3 and 1.37×10^{15} atoms/cm^3 are shown, with the results of hydrogen-annealed wafers and argon-annealed wafers respectively superimposed. Also, in Figure 7, the results of the wafers of Figure 5(A) to Figure 6(C) are shown superimposed.

From these results, it appears that there is an upper limit in the results of performing the constant-current TDDB test on nitrogen-doped argon-annealed wafers between nitrogen concentrations of 1.64×10^{14} atoms/cm^3 (Figure 6(A)) and 5.82×10^{14} atoms/cm^3 (Figure 6(B)); this is present at a location close to the value of 4×10^{14} atoms/cm^3 (Figure 6(D)), which was deemed to be the upper limit from the results of performing the constant-current TDDB test for hydrogen-annealed wafers.

From the above, it can be seen that, although there is a big difference in the results of the TZDB test between hydrogen-annealed and argon-annealed nitrogen-doped wafers, there is scarcely any difference in terms of the results of the constant-current TDDB test.

Thus, from the fact that, for silicon wafers for semiconductor devices (silicon wafers for manufacturing semiconductor devices), the results of the TDDB test must be seriously taken into account, it can be seen that nitrogen-doped wafers for non-oxidative heat treatment that are to be the subject of hydrogen annealing or argon annealing must in each case contain nitrogen with a concentration of 4×10^{14} atoms/cm^3 or less, which is considered to be the upper limit from the results of a constant-current TDDB test.

Figure 8 is a view showing the change of nitrogen concentration in a pulled single crystal when pulled by the CZ method. In this Figure 8, the horizontal axis shows the solidification ratio, taking the total amount of polysilicon raw material, which is the raw material of the single crystal ingot, which is introduced as 1, while the vertical axis shows the nitrogen concentration. In this Figure, (a) is the curve when the initial concentration is 2 X 10^{14}, and (b) is the curve when the initial concentration is 1 X 10^{14} and (c) is the curve when the initial concentration is 5 X 10^{13}.

As is clear from this Figure 8, due to the nitrogen segregation phenomenon, the nitrogen concentration becomes higher towards the tail end of the pulled silicon ingot (the corresponding silicon ingot shape is shown on the graph).

INDUSTRIAL APPLICABILITY

As described above, according to the present invention, a nitrogen-doped silicon wafer can be provided showing excellent wafer characteristics for a product.

CLAIMS

1. A silicon wafer for non-oxidative heat treatment for use in semiconductor device manufacture, wherein nitrogen concentration is in the range from 5 X 10^{13} atoms/cm^3 to 1 X 10^{15} atoms/cm^3.

2. A silicon wafer for non-oxidative heat treatment for use in semiconductor device manufacture, wherein nitrogen concentration is in the range from 5 X 10^{13} atoms/cm^3 to 4 X 10^{14} atoms/cm^3.

3. A silicon wafer for non-oxidative heat treatment for use in semiconductor device manufacture according to any one of claim 1 and claim 2, wherein the silicon wafer is a silicon wafer for hydrogen heat treatment or a silicon wafer for argon annealing.

4. A method of manufacturing a silicon ingot for manufacturing of silicon wafers for non-oxidative heat treatment, wherein in a method of manufacturing a silicon ingot by pulling a silicon single crystal by Czochralski method, nitrogen is doped and the silicon single crystal is pulled under a condition that a portion is formed in which nitrogen concentration is from 5 X 10^{13} atoms/cm^3 to 1 X 10^{15} atoms/cm^3.

5. A silicon wafer for manufacturing a semiconductor device manufactured by hydrogen heat treatment or argon annealing of the silicon wafer for non-oxidative heat treatment according to any of claim 1 to claim 3.

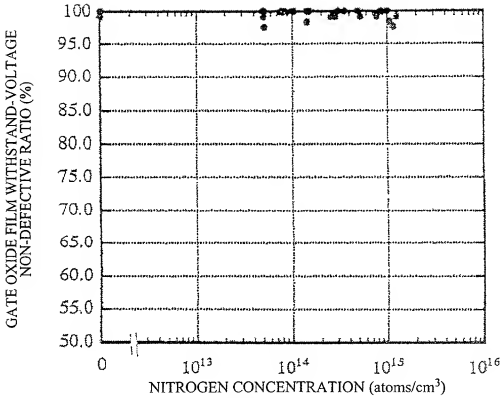
6. A silicon wafer for semiconductor device manufacture wherein doping amount of nitrogen is adjusted taking into account life of a virtual element.

7. A method of evaluating a nitrogen-doped wafer wherein decision as to whether or not the nitrogen-doped wafer can be used as a wafer for semiconductor device manufacture is made by calculating life of a virtual element on a nitrogen-doped heat treatment wafer.

8. The method of evaluating wafers according to claim 7 wherein the method of calculating the life of the virtual element on the wafer is the TDDB test.

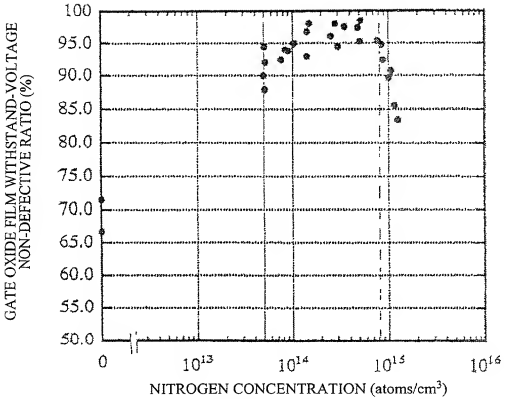
ABSTRACT

A method for producing a silicon ingot through pulling up a silicon single crystal according to the Czochralski method, wherein the silicon single crystal is pulled up while being doped with nitrogen in such a condition as to form a part having a nitrogen content of 5 X 10^{13} atoms/cm^3 to 1 X 10^{15} atoms/cm^3. A silicon wafer having a nitrogen content of 5 X 10^{13} atoms/cm^3 to 1 X 10^{15} atoms/cm^3 which is suitable for being treated with heat in a non-oxidizing atmosphere is manufactured of an ingot produced by using the method. The method can be used for producing a silicon wafer being doped with nitrogen and having satisfactory characteristics for use in a semiconductor device.



RELATIONSHIP BETWEEN ADDED NITROGEN CONCENTRATION AND OXIDE FILM WITHSTAND-VOLTAGE NON-DEFECTIVE RATIO AFTER HYDROGEN ANNEALING

FIG.1



RELATIONSHIP BETWEEN ADDED NITROGEN CONCENTRAION AND OXIDE FILM WITHSTAND-VOLTAGE NON-DEFECTIVE RATIO AFTER REMOVAL BY POLISHING SURFACE LAYER OF 3 μm AFTER HYDROGEN ANNEALING

FIG.2

HYDROGEN ANNEALING (NON-DOPED)

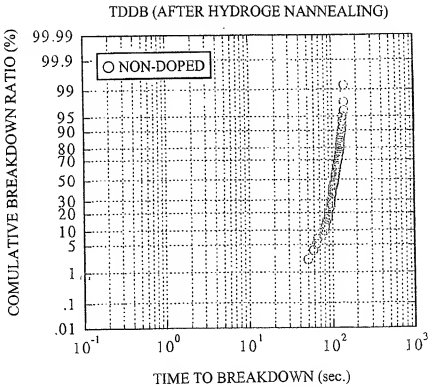


FIG.3(A)

HYDROGEN ANNEALING (N = 5.82E14)

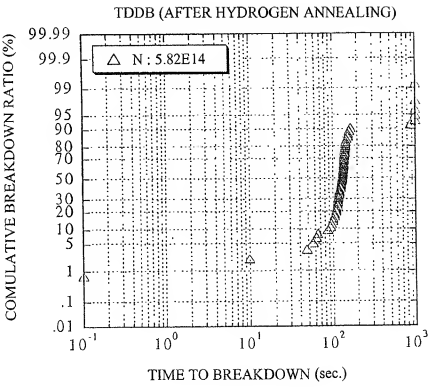


FIG.3(B)

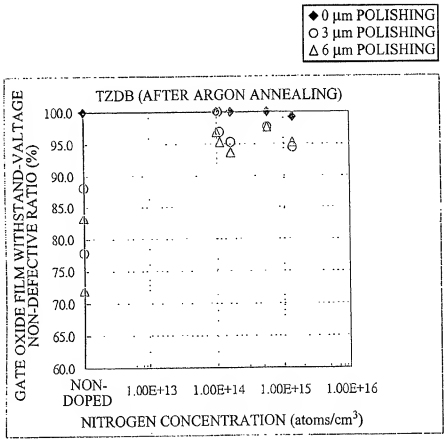


FIG.4(A)

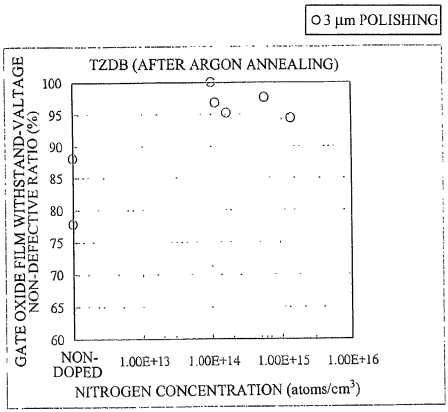


FIG.4(B)

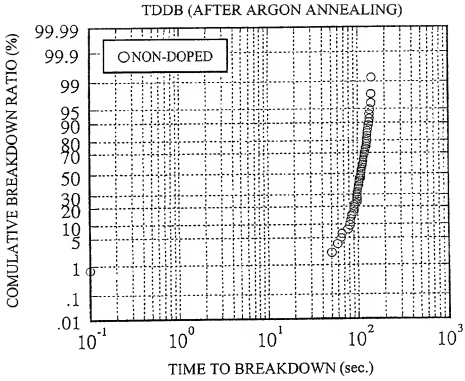

TDDB (AFTER ARGON ANNEALING)
NON-DOPED
COMULATIVE BREAKDOWN RATIO (%)
99.99
99.9
99
95
90
80
70
50
30
20
10
5
1
.1
.01
10^{-1}
10^{0}
10^{1}
10^{2}
10^{3}
TIME TO BREAKDOWN (sec.)

FIG.5(A)

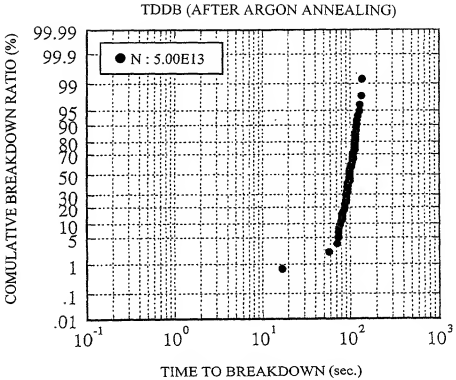


FIG.5(B)

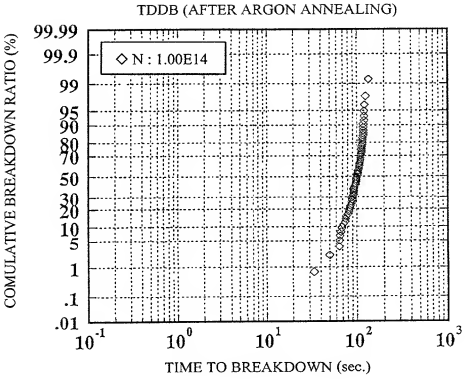


FIG.5(C)

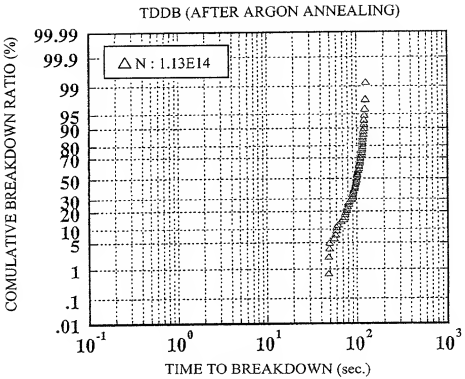


FIG.5(D)

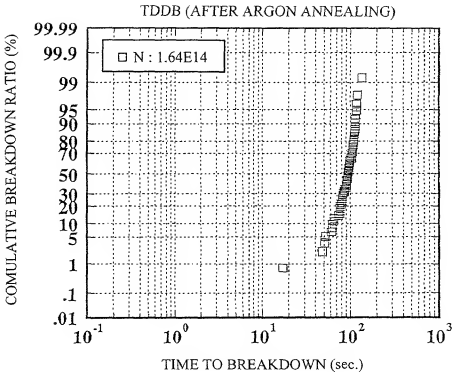

TDDB (AFTER ARGON ANNEALING)
N : 1.64E14
COMULATIVE BREAKDOWN RATIO (%)
99.99
99.9
99
95
90
80
70
50
30
20
10
5
1
.1
.01
10^{-1}
10^{0}
10^{1}
10^{2}
10^{3}
TIME TO BREAKDOWN (sec.)

FIG.6(A)

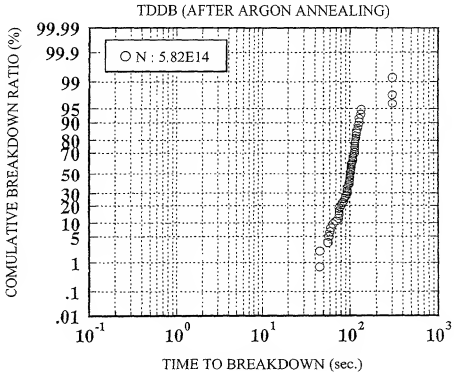


FIG.6(B)

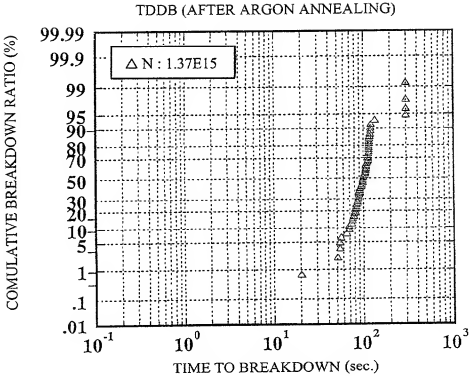


FIG.6(C)

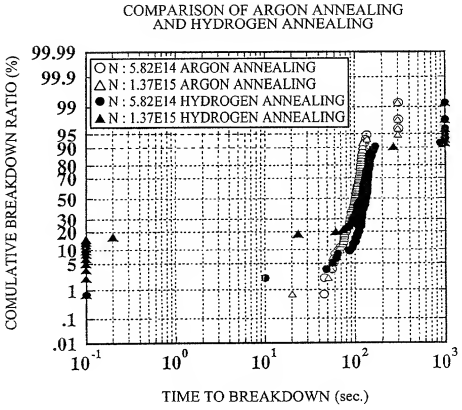


FIG.6(D)

ANNEALING CONDITIONS : 1200C, 1.0hr IN 100% Ar

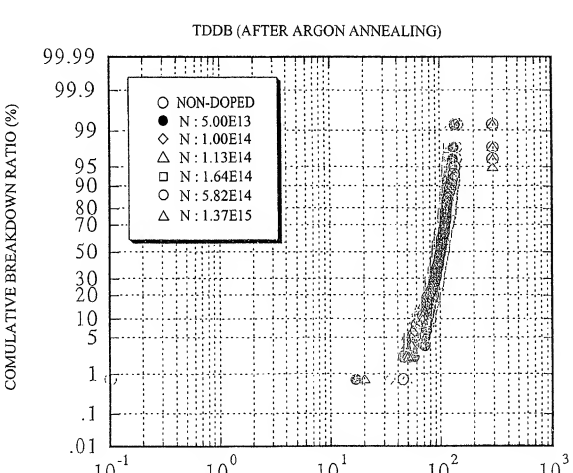


FIG.7

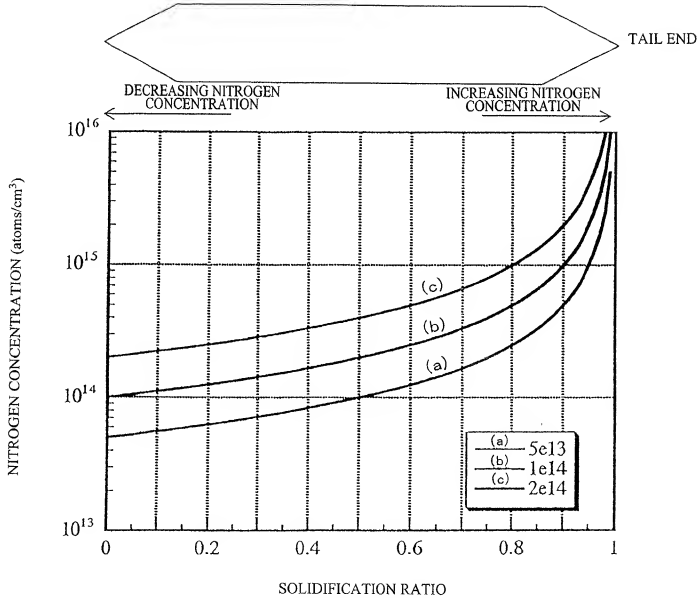


FIG.8

FEM-109US

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare:

That my residence, post office address and citizenship are as stated below next to my name.

That I verily believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: SILICON WAFER AND METHOD FOR MANUFACTURE THEREOF, AND METHOD FOR EVALUATION OF SILICON WAFER the specification of which (check one)

☐ is attached hereto.

☒ was filed on August 25, 2000 as Application, Serial No. PCT/JP00/05738 and was amended on ______ (if applicable).

That I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

That I acknowledge the duty to disclose information known to be material to patentability of this application in accordance with Title 37, Code of Federal Regulations §1.56(a).

That I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate on this invention having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

(Number)	(Country)	(Day/Month/Year Filed)	Priority Claimed
241186/1999	Japan	27/8/1999	☒ Yes ☐ No
			☐ Yes ☐ No

That I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

United States Application(s)

(Application Serial No.)	(Filing Date)	(Status)-(Patented, pending, abandoned)

KEM-10903

That all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

I hereby appoint the following attorneys, with full power of substitution and revocation, to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith and request that all correspondence and telephone calls in respect to this application be directed to: WELSH & KATZ, LTD., 120 South Riverside Plaza, 22nd Floor, Chicago, Illinois 60606-3913, Telephone No.: (312) 655-1500:

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